Analysis of Area Efficiency of 12-bit Switched-Capacitor DAC Topologies used in SAR ADC

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Abstract—In this paper we present analysis of area efficiency of conventional binary-weighted and split-capacitor topologies of switched-capacitor DAC for SAR ADC. Although the main reason for usage of split-capacitor topologies is reducing the DAC's area, the analysis showed that it is not always the case since the linearity parameters of split-capacitor topologies are more sensitive to parasitic effects. We based our analysis on differential realization of 12-bit switched capacitor digital-to-analog converter for 1 MS/s differential SAR ADC in 180 nm CMOS. However, the analysis can be applied to any SC DAC used in SAR ADCs. We used common mode voltage as a third reference voltage potential besides *GND* and V_{REF}, which allowed us to reduce the DAC's area while maintaining the linearity specifications. Monte Carlo simulations of the designed DAC with extracted parameters gave the 12-bit performance at 1 MS/s with the differential nonlinearity in LSBs $DNL_{max,mean}/\sigma_{DNLmax} = +0.395/0.201$ and integral nonlinearity $INL_{max,mean}/\sigma_{INLmax} = +0.326/0.108$.

Index Terms—Switched capacitor DAC, SAR ADC, differential DAC array, MIM capacitors, mismatch.

I. INTRODUCTION

SUCCESSIVE approximation register analog-to-digital converters (SAR ADC) [1] are widely used in low power and medium-resolution applications such as medical implant devices [2], wireless sensor networks [3], etc. One of the key elements of every SAR ADC is the digital-to-analog converter (DAC).

The DAC in SAR ADC is usually based on the switched resistors network, switched current sources network or switched capacitors network. The latter is convenient for low power applications since it does not consume static power like the former ones. Also, the switched capacitor DAC network can be used as the sample and hold circuit in the sample phase. Differential realizations of SAR ADC, compared to single-ended realizations, are more resistant to noise and other effects which reduce the ADC's performance such as charge injection. These realizations require two switched capacitor arrays: one for positive, and another for negative comparator input which can increase the chip area.

There are multiple studies on capacitor array topologies [4], [5] and switching algorithms [6], [7] that discuss converter's linearity, energy efficiency, performance and area problems. The SAR ADC's performance depends on multiple parameters like technology parameters, supply voltage, unit capacitors size etc. This paper describes a

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design of the 12-bit switched capacitor DAC for differential SAR ADCs in 180 nm CMOS technology with the detailed analysis of area efficiency of different topologies.

In most cases, the switched capacitor network is binary-weighted capacitor array. It can be divided to sub-arrays using split capacitor technique in order to avoid large capacitance differences, and hopefully achieve smaller total area [4], [5]. We have investigated these two most commonly used switched capacitor topologies: with and without split capacitor. We analyzed how these different capacitor networks are influenced by capacitor mismatch, parasitic capacitances, charge injection and kT/C noise. Based on this analysis, we chose the minimal unit capacitance for each of these topologies in order to meet acceptable error level for 12-bit performance. We show that since the split capacitor topology is more sensitive to aforementioned parasitic effects, larger unit capacitor must be used and in some cases can produce even larger total area than simple binary-weighted capacitor network.

In the next section, we describe the effects that influence the DAC's performance and choose the topology for our differential DAC. Some layout considerations are presented in the section III, while the section IV presents the results of post-layout simulations. In the end, we summarize our results and give conclusions and proposals for further work in the section V.

II. CHOOSING THE DAC TOPOLOGY

A. Binary-weighted capacitive array topologies

The differential DAC is consisted of two identical binary-weighted capacitive arrays. In our 12-bit differential DAC, we use two 11-bit single-ended capacitive arrays since we use a common mode voltage V_{CM} as a third reference voltage besides *GND* and V_{REF}. Detailed explanation will be given in the subsection II.C. Therefore, it is enough to analyze an 11-bit single-ended capacitive array in order to determine the best topology. In our design, we used metal-insulator-metal (MIM) capacitors available in our 180 nm CMOS technology library.

Fig. 1.a) shows a single-ended DAC which is consisted of binary-weighted capacitor array where the capacitance which corresponds to the DAC bit i is two times larger than the capacitance which corresponds to the DAC bit $i-1$. C_U is the unit capacitance, while red C_p capacitors model top plate parasitic capacitances which have influence on DAC gain and linearity. The unit capacitance C_U should be as small as possible in order to achieve small area, small power consumption and/or high speed. However, mismatch effects that occur due to the imperfect technology process are more expressed when using small capacitance values and

therefore have higher influence on the DAC nonlinearity. Mismatch effects of two identical MIM capacitors which are close to each other are usually modeled using the following expression

$$\sigma\left(\frac{\Delta C}{C}\right) = \sigma(\delta C) = \frac{K_\sigma}{\sqrt{A}}, \qquad (1)$$

where A is the capacitor's area and K_σ is the matching coefficient. Our technology has the matching $K_\sigma = 2.51\ \%\mu m$.

Unit capacitor is modeled with its capacitance C_U and its standard deviation σ_U which represents the mismatch effects. For single MIM capacitor the expression σ_U/C_U is $\sqrt{2}$ times smaller than $\sigma(\delta C_U)$. The standard deviation of differential and integral nonlinearity of the binary-weighted capacitor array is determined by these parameters and by the DAC's number of bits. According to the analysis from [8] the standard deviation of the maximal differential nonlinearity of N-bit DAC can be expressed as

$$\sigma_{DNL\,max} = \sqrt{2^N - 1}\,\frac{\sigma_U}{C_U}\,LSB, \qquad (2)$$

while the standard deviation of the maximal integral nonlinearity of N-bit DAC can be expressed as

$$\sigma_{INL\,max} = \sqrt{2^{N-1}}\,\frac{\sigma_U}{C_U}\,LSB. \qquad (3)$$

It is obvious that the $\sigma_{DNL\,max}$ is more restrictive parameter and it is used as a reference for the calculation of the lower bound for the unit capacitance value. Therefore, it is necessary to maintain $3\sigma_{DNL\,max} < 1/2\,LSB$. This leads us to the expression for the unit capacitance value in conventional binary-weighted topology

$$C_{U,\,bw} > 18 \cdot \left(2^N - 1\right) \cdot K_\sigma^2 K_C. \qquad (4)$$

In the previous equation, the K_C is the capacitance density parameter from the capacitance equation $C = K_C A$ and for our technology it is equal to 2 fF/μm^2.

In the differential topology, the C_U can have two times smaller value while maintaining the same linearity. This is the case since the LSB is two times larger while the error voltage introduced by the mismatch is only $\sqrt{2}$ times larger than in single-ended topology. Finally we get the minimum unit capacitance for differential topology

$$C_{Ud,\,bw} > 9 \cdot \left(2^N - 1\right) \cdot K_\sigma^2 K_C. \qquad (5)$$

Using the (5), we can determine the unit capacitance and for our technology $C_U > 23.21$ fF. However, for single-ended N-bit DAC we need 2^N unit capacitors that take large area. This number is even larger since dummy capacitors need to be placed all around the capacitors array. Dummy

capacitors improve the cancellation of the fringe capacitance mismatch influence since the fringe capacitance at edges of the capacitor bank is the same as that within the bank. We can estimate the number of dummy capacitors to $4 \cdot 2^{N/2} + 4$ if the capacitors array is squared. Hence, the total number of unit capacitors is

$$Num_{C,\,bw} = 2^N + 2^{N/2+2} + 4. \qquad (6)$$

In order to reduce the number of unit capacitors, the split capacitor technique is commonly used [4]. The DAC array where the capacitive array is divided to two sub-arrays using the bridge capacitor C_B is shown in Fig. 1.b), where S is the number of bits in the LSB sub-array, M is the number of bits in the MSB sub-array and $N = S + M$. In order to achieve equivalent bit weights as in conventional binary-weighted array, the bridged capacitor capacitance needs to be

$$C_B = \frac{2^S}{2^S - 1}\,C_U. \qquad (7)$$

This capacitance value is inconvenient for matching with other capacitors since it has a fractional part of C_U.
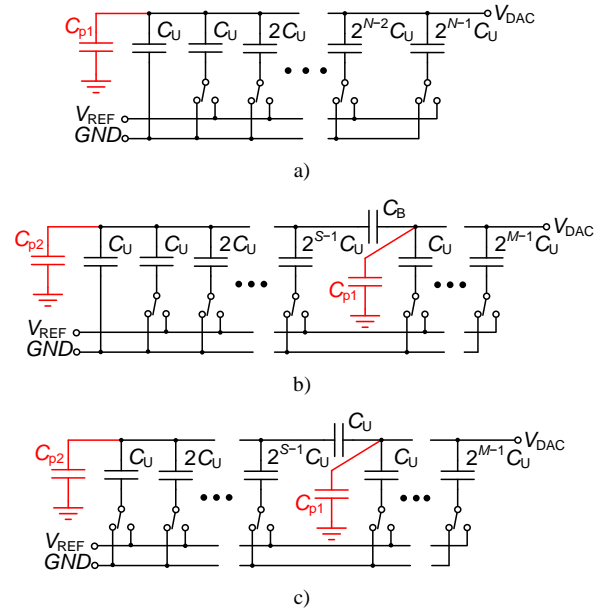

Fig. 1. Single-ended capacitor array topologies. C_U is the unit capacitance, while red C_p capacitors model parasitics. a) Binary-weighted capacitor array. b) Split binary-weighted capacitor array. c) Modified split binary-weighted capacitor array to avoid fractional value of the bridge capacitor.

The modified split-capacitor DAC array [5] is shown in Fig. 1.c) where a single unit capacitor is used as a bridge capacitor, but the dummy unit capacitor is removed. This topology induces the gain error of $1/\left(1 - 2^{-N}\right)$ which is linear and can be easily compensated.

Using the analysis from [8] and with maintaining the $3\sigma_{DNL\,max} < 1/2\,LSB$ we can derive the minimum unit capacitance for the modified split-capacitor differential topology

$$C_{Ud,\,split} > 9 \cdot \left(2^M - 1\right) \cdot 2^{2(N-M)} K_\sigma^2 K_C. \qquad (8)$$

This value is larger than the value of the unit capacitance for the conventional binary-weighted array.

The number of unit capacitors in the single modified split-capacitor array is

$$Num_{C,\,split} = 2^S + 2^M - 1 + Num_{C,\,dummy}, \qquad (9)$$

where $Num_{C,\,dummy}$ is determined in the similar way like in (6)

$$Num_{C,\,dummy} = 4\left\lceil \sqrt{2^S + 2^M - 1} \right\rceil + 4. \qquad (10)$$

The total capacitive array area is determined by the area of the single unit capacitor and by the number of unit capacitors. Additional overhead due to the DRC rules must be added to this area. The overhead is larger as the unit capacitance is smaller since less area is used for capacitance and more for capacitor contacts and empty space needed because of DRC. Fig. 2 shows this overhead area. The total area occupied by a single unit capacitor due to the capacitor area and vertical and horizontal overhead, according to the Fig. 2, can be expressed as

$$A_{C_U,\,total} = \left(\sqrt{A_{C_U}} + VO\right)\cdot\left(\sqrt{A_{C_U}} + HO\right). \qquad (11)$$
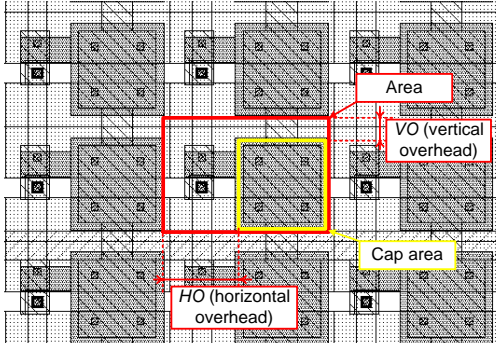

Fig. 2. MIM capacitors layout with the overhead area for DRC and capacitor contacts

In order to determine area savings in modified split-capacitor topology we calculate the parameter $R(M)$ which is the ratio of the total needed area for the split-capacitor topology and the total needed area for the conventional binary-weighted topology for different values of M.

$$R = \frac{Num_{C,\,split}\cdot A_{C_U,\,total,split}}{Num_{C,\,bw}\cdot A_{C_U,\,total,bw}}$$
$$= \frac{Num_{C,\,split}\left(\sqrt{CR\cdot A_{C_U,\,bw}} + VO\right)\left(\sqrt{CR\cdot A_{C_U,\,bw}} + HO\right)}{Num_{C,\,bw}\left(\sqrt{A_{C_U,\,bw}} + VO\right)\left(\sqrt{A_{C_U,\,bw}} + HO\right)}, \qquad (12)$$

where CR is the unit capacitances ratio

$$CR = \frac{C_{Ud,\,split}}{C_{Ud,\,bw}} = \frac{9\cdot\left(2^M - 1\right)\cdot 2^{2(N-M)} K_\sigma^2 K_C}{9\cdot\left(2^N - 1\right)\cdot K_\sigma^2 K_C}, \qquad (13)$$

which provides the same $\sigma_{DNL\,max}$ for both topologies.

Fig. 3 shows a plot of parameter $R(M)$ for minimal

$A_{C_U,\,bw}$ in our 180 nm CMOS technology library for 11-bit capacitive array. We give results for 11-bit single-ended capacitive DAC since it is used in our differential DAC to achieve the 12-bit resolution. As can be seen in Fig. 3, for our application, the largest area savings are 30 % for $M = 8$.
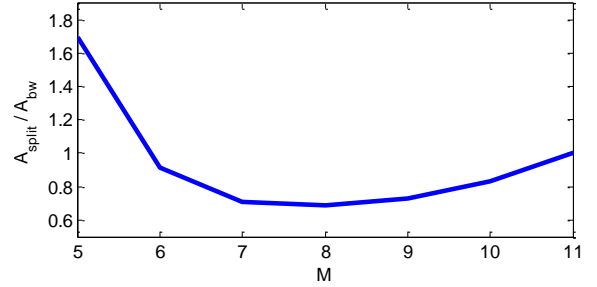

Fig. 3. Area savings due to usage of modified split-capacitor topology for different values of bit number in the MSB array M.

Here, we need to consider the influence of top plate parasitic capacitances on the linearity. In Fig. 1 these parasitic capacitances are modeled as additional capacitors C_{p1} and C_{p2}. According to [9], the capacitance C_{p2} has strong influence on the DAC linearity. In order to reduce its influence, the capacitance C_{p2} needs to be as small as possible. It is composed of top plate parasitic capacitances in the LSB array and the top plate parasitic capacitance of the bridge capacitor and can be expressed as following

$$C_{p2} = \alpha\left(C_{sumLSB} + C_B\right) = \alpha\left(\sum_{i=0}^{S-1} 2^i C_U + C_U\right) = \alpha 2^S C_U, \quad (14)$$

where α is the percentage of the top-plate parasitic capacitance. Based on [9] we can write expression for the output voltage of the DAC if the input code is $B = b_N...b_0$

$$V_{DAC}(B) = \frac{C_B\left(\sum_{i=0}^{S-1} b_i 2^i C_U + \sum_{i=0}^{M-1} b_{i+S} 2^i C_U\right)}{C_{denom}} V_{ref} + $$
$$\frac{\left(C_{sumLSB} + C_{p2}\right)\sum_{i=0}^{M-1} b_{i+S} 2^i C_U}{C_{denom}} V_{ref}, \qquad (15)$$

where C_{denom} is $C_B(C_{sumLSB} + C_{sumMSB} + C_{p1} + C_{p2}) + (C_{sumLSB} + C_{p2})(C_{sumMSB} + C_{p1})$. C_{sumMSB} is the total capacitance of the MSB sub-array. Hence, the LSB value is

$$LSB = \frac{V_{DAC}(2^N - 1)}{2^N - 1} = \frac{C_U^2(2^N - 1) + C_U C_{p2}(2^M - 1)}{C_{denom}} V_{ref}. \quad (16)$$

Using expressions (15) and (16) we can derive the expression for maximal differential nonlinearity of 11-bit single-ended DAC which comes from parasitic capacitances

$$DNL_{maxp} = \frac{V_{DAC}(1024) - V_{DAC}(1023)}{LSB} - 1$$
$$= \frac{\left(C_U + C_{p2}\right)\left(2^N - 1\right)}{C_U(2^N - 1) + C_{p2}(2^M - 1)} - 1. \qquad (17)$$

As we can see from (17) reducing the number of capacitors in the MSB array leads to the increased nonlinearity. This is why we need to modify the condition $3\sigma_{DNL\max} < 1/2\,LSB$ to the $3\sigma_{DNL\max} < 1/2\,LSB - DNL_{\max p}$ when derive the minimal capacitance of the unit capacitor. This will modify the capacitances ratio in (12) to

$$CR_{\mathrm{p}} = \frac{9 \cdot \left(2^M - 1\right) \cdot 2^{2(N-M)} K_\sigma^2 K_C}{9 \cdot \left(2^N - 1\right) \cdot K_\sigma^2 K_C} \cdot \left(\frac{0.5}{0.5 - DNL_{\max p}}\right)^2 . \quad (18)$$

Fig. 4 shows modified area ratio for different values of parameter α. As we can see, if parasitic effects are more expressed, there is no area saving when using the split-capacitor topology at all if the linearity is kept unchanged compared to the conventional binary-weighted capacitive array.
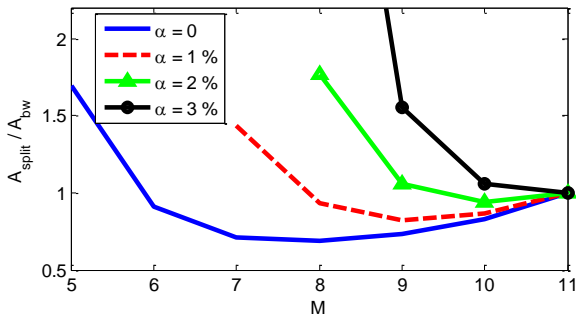

Fig. 4. Modified area savings from Fig. 3. when top-plate parasitics are considered for different values of parasitics percentage α.

Parasitic extraction showed that in our technology the parameter α is around 1 %, which would lead us to the usage of the split-capacitor topology with $M = 9$. However, the minimal available capacitance in the technology library is 35.6 fF, hence the ratio given in (12) (for $CR = CR_{\mathrm{p}}$) and in Fig. 4 is the ratio for even more restrictive $3\sigma_{DNL\max}$ than the $1/2\,LSB$. For conventional binary-weighted capacitive array topologies, we can put two capacitors in series for LSB and dummy capacitor in order to achieve two times smaller equivalent capacitance. In that case the additional mismatch effects need to be considered and the case would be the same as in (8) for $M = 10$. The minimal unit capacitance which provides the $3\sigma_{DNL\max}$ rule is now 48.3 fF. The total capacitive array area in this case, which is the new reference, is only 3.3% larger than minimal total capacitive array area achievable for $M = 9$. This is the reason why we decided not to use the architecture with the bridge capacitor.

In the end, we analyzed what would happen if we use the minimal possible capacitor of 35.6 fF as unit capacitor instead of the capacitor of capacitance 48.3 fF. In this case $1/2\,LSB - DNL_{\max p} > 2.5\sigma_{DNL\max}$ which gives us the probability of 98.8% that the $DNL_{\max}$ due to mismatch effects would be less than $1/2\,LSB$. This is only 0.9 % less than the probability for the $3\sigma_{DNL\max}$, hence we decided to use the minimal capacitor available in our 180 nm CMOS technology for DAC capacitive array.

B. Bottom plate sampling

Sampling circuits consist of a sampling capacitor and a switch made out of transistor/s. Whenever a transistor is turned off, the channel charge is injected into the nodes connected to drain and source. Injected charge induces the voltage error on the sampling capacitor which is dependent on the input voltage [10]. This effect makes the dynamic offset which degrades the ADC performance.

In order to reduce the charge injection effects multiple solutions were proposed [11], [12], but the most effective one is the bottom plate sampling [12]. Fig. 5 shows simplified scheme which realizes this method. The sampling capacitor is connected to two switches: switch φ_1 which is the sampling switch and switch φ_2 which connects the top plate of the capacitor to the constant voltage potential. The sampling capacitor is disconnected from the input voltage using the switch φ_2 and charge injection comes only from this switch. Since the switch φ_2 is connected to the constant voltage potential, the injected charge is always the same. Using this scheme, only a static offset is added to the input signal which is cancelled using the differential architecture. The timing diagram of switches activity is shown in Fig. 5.
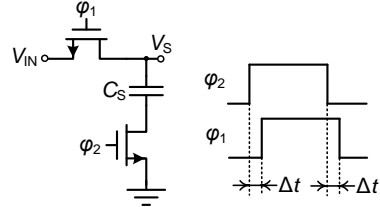

Fig. 5. Bottom plate sampling switches and the timing diagram of the control signals.

C. Proposed differential DAC

Using the binary-weighted capacitive array topology from subsection II.A and bottom plate sampling we present the architecture of our 12-bit DAC in Fig. 6. As mentioned before, we use the common mode voltage $V_{CM} = V_{REF}/2$ as a third reference voltage. Capacitors C_0 and C_1 are consisted of two serially connected unit capacitors.
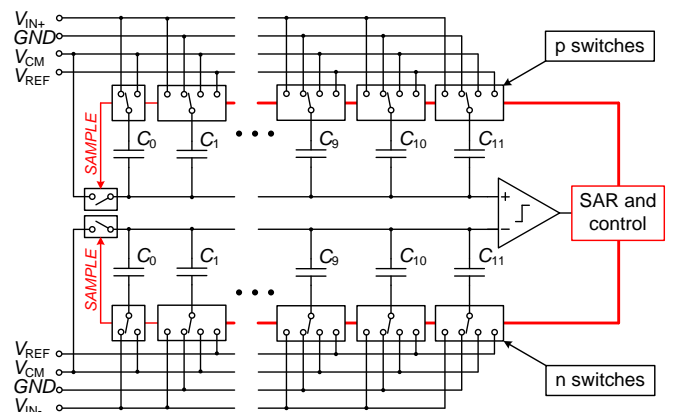

Fig. 6. A block diagram of the proposed differential DAC

In the sampling phase, all bottom plates of the capacitors are connected to V_{IN+}/V_{IN-} nodes, while top plates are connected to the V_{CM} node. After the sampling phase, the sample switch is turned off, and all bottom plates are connected to the V_{CM}. Now, the input voltage of the analog comparator is $V_+ - V_- = -V_{IN}$ and the sign of the input

voltage is determined. If the comparator output is 1, the input signal is negative, otherwise it is positive. The sign bit determines which reference voltage (V_{REF} or *GND*) will be further used in top and which in bottom capacitive array. After the sign is determined, all other bits are determined using standard successive approximation algorithm. The output code of the SAR ADC is the signed magnitude representation of the digital value.

Switch boxes structure used in the DAC is shown in Fig. **7**. In order to achieve the sample rate of 1 MS/s switches for C_8, C_9, C_{10}, and C_{11} are 2, 4, 8, and 16 times larger than switches for C_{7-0} respectively.

Switch logic in n switches:

$P = \overline{SIGN \cdot SAMPLE} \cdot b_i$
$Q = \overline{SAMPLE} + b_i$
$R = \overline{\overline{SIGN} \cdot SAMPLE} \cdot b_i$
$S = SAMPLE$

Switch logic in p switches:

$P = \overline{SIGN \cdot SAMPLE \cdot b_i}$
$Q = SAMPLE + b_i$
$R = \overline{SIGN} \cdot \overline{SAMPLE} \cdot b_i$
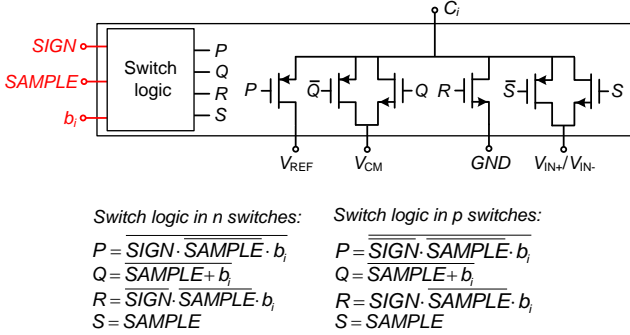$S = SAMPLE$

Fig. 7. Switch box used in the differential DAC. Logic functions that generate signals at transistor gates are slightly different for switch boxes in positive and negative capacitive array.

D. kT/C noise influence

Thermal noise in switched capacitors circuits mainly comes from switches that behave like resistors and induce thermal noise of power spectral density $\overline{v_n^2} = 4kTR_{on}$, where k is Boltzmann's constant, T is absolute temperature and R_{on} is the equivalent resistance of turned-on switch. When used in switched capacitor circuits, the thermal noise is filtered on the RC filters that come from the switch resistors and capacitors. The simplest example is the sampling shown in Fig. 8.a). The switch is modeled using the noiseless resistor of resistance R_{on} and the voltage source of thermal noise. The equivalent noise power of filtered noise at the output is $v_{n,out}^2 = kT/C$ and is independent from the switch resistance [13].

All switches in the switched capacitor array induce thermal noise and the total noise power at the comparator input can be determined using the superposition.

At one comparator input, the top plate sampling switch induce the noise of power $v_{n,comp+/-}^2 = kT/C_{total}$, where C_{total} is the total capacitance of the capacitive array. Fig. 8.b) shows the equivalent circuit for calculation of bottom plate switches contributions. The capacitor C_1 is the capacitor to which the switch is connected, while the C_2 is the capacitance of all other capacitors. The total noise power from bottom plate switches in the binary-weighted capacitor array is the sum of all contributions which are calculated like in Fig. 8.b). The capacitance C_1 for switch box i is $C_1 = 2^{i-1}C_U$ for $i = 1, 2, …, 11$ and $C_1 = C_U$ for $i = 0$, while the capacitance C_2 is $C_2 = 2048C_U - C_1$.

Following this procedure we can calculate the total noise power at the output of the differential DAC. For our unit capacitance of 35.6 fF/2 = 17.8 fF the total noise power is
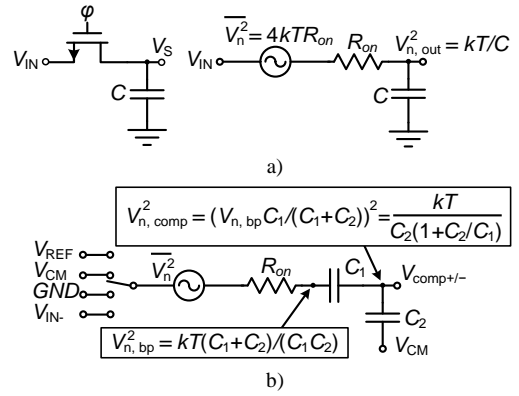

a)

b)

Fig. 8. a) Sampling circuit example and equivalent circuit for calculation of thermal noise influence. b) Equivalent circuit for calculation of bottom switches contribution on the thermal noise at the comparator input.

592 μV^2 which gives the RMS voltage of $V_{n,rms} = 24.33\,\mu V$. If the V_{REF} is 1.8 V, the *LSB* is 879 μV. Therefore, we further considered that the influence of the kT/C noise is insignificant when compared with previous error sources.

E. Other error sources

Besides the charge injection effect, switches induce a clock feedthrough error. It is manifested as an input-independent error and therefore can be treated as offset error which does not influence linearity performance [5].

In order to achieve the proper track bandwidth we propose the sampling phase which is three times longer than the one step of the conversion phase. This is necessary due to the additional resistance of the top plates switch.

III. LAYOUT CONSIDERATIONS

We designed the layout of the capacitive array using the partial common-centroid configuration presented in [14] in order to simplify the routing and hence reduce the parasitic effects. The capacitors C_{11-6} are placed in common-centroid configuration while other capacitors are placed in the middle of the capacitive array but without using the common-centroid configuration. The layout of a single capacitive array drawn in *Cadence Virtuoso LE* is shown in Fig. 9.

In order to reduce the gain mismatch between top and bottom capacitive arrays, a we placed a shield in metal 4 bellow MIM capacitors of both arrays and connected it to
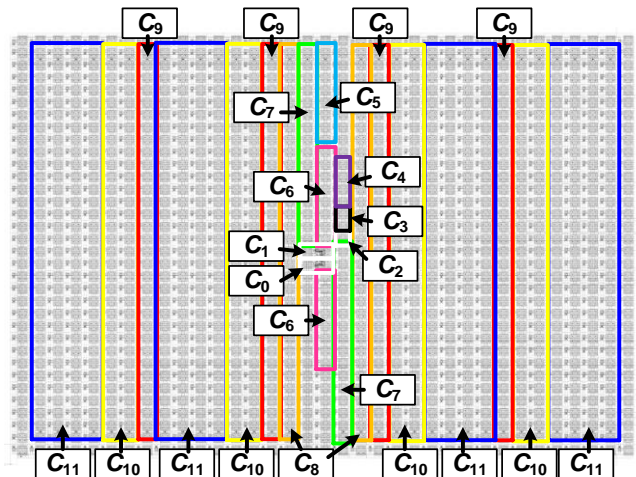

Fig. 9. The layout of the single ended capacitive array designed using the partial common-centroid configuration.

the V_{CM} reference. The shield is connected to V_{CM} because it is used in both DAC arrays as the voltage to which capacitors are connected if their corresponding bit is 0.

IV. SIMULATION RESULTS

The proposed DAC has total capacitance of 36.5 pF per array and takes total area of 0.144 mm^2 including the switch boxes and capacitive arrays.

Fig. 10 shows the differential and integral nonlinearity. We obtained results by running 1000 Monte Carlo simulations of the differential DAC after the parasitic extraction. Fig. 10.a) shows the mean value of the differential nonlinearity obtained in these simulations. The maximum *DNL* is for the input codes +1024 and −1024 and the mean value of it is $DNL_{max} = +0.395$. Fig. 10.b) shows the mean value of the integral nonlinearity. The maximum *INL* is $INL_{max} = 0.326$. Fig. 10.c) and Fig. 10.d) show standard deviations of the differential nonlinearity and the integral nonlinearity whose maximum values are $\sigma_{DNL\,max} = 0.201$ and $\sigma_{INL\,max} = 0.108$.
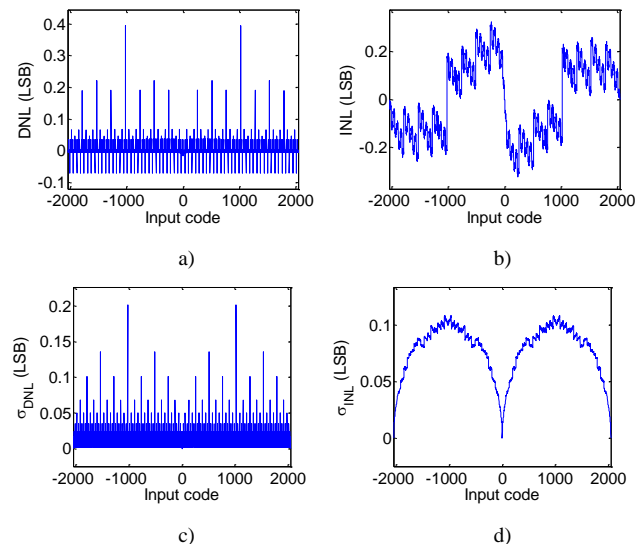

Fig. 10. Mean values and standard deviations of differential and integral nonlinearity of the DAC.

Results show that the routing parasitics influence on the linearity is large, although the DNL_{max} is less than 1 LSB in worst case, which provides the monotonic DAC transfer function and prevents missing codes.

Technology parameters very much contribute to the performance results since the MIM capacitors mismatch of 2.51 % µm is large compared with modern CMOS technologies.

Further improvements of the DAC linearity can be done by even more careful layout design and potentially using other switching algorithms like in [6] and [7].

V. CONCLUSION

In this paper we presented detailed analysis of parasitic effects in different switched capacitor DAC topologies and analyzed their influence on the minimum unit capacitance value as well as on the total capacitive array area. We showed that, although the split-capacitor topologies have the main contribution in reducing the capacitive array area, the

area savings are not always followed with the performance and linearity preservation. As an example, we presented one realization of the differential 12-bit DAC for SAR ADC. The DAC is designed as the differential binary-weighted capacitive array using MIM capacitors.

The results show that 12-bit resolution when using the minimum capacitor available in our 180 nm CMOS technology is almost the limiting resolution for SAR ADCs with switched capacitor DAC in this technology without calibration or compensation circuits.

Our further work included the design of the analog comparator and digital logic for the proposed SAR ADC. We believe that additional investigations on the DAC topologies can be done when using other switching algorithms too.

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